Figure 1(a). Gate to common short defects in TFT array with double common line layout.

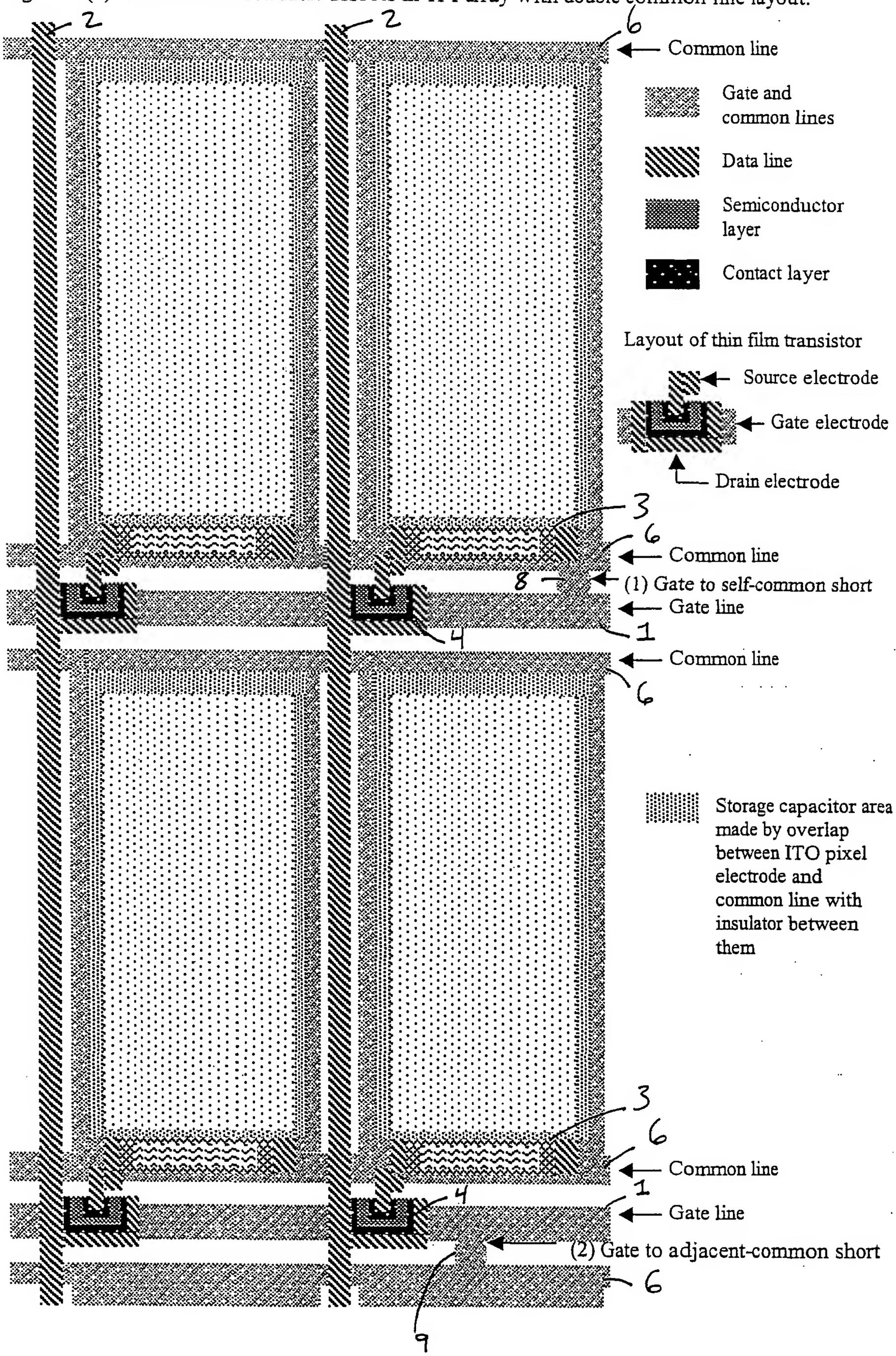


Figure 1(b). Explanation of pixel layout by showing four pixels in different process step.

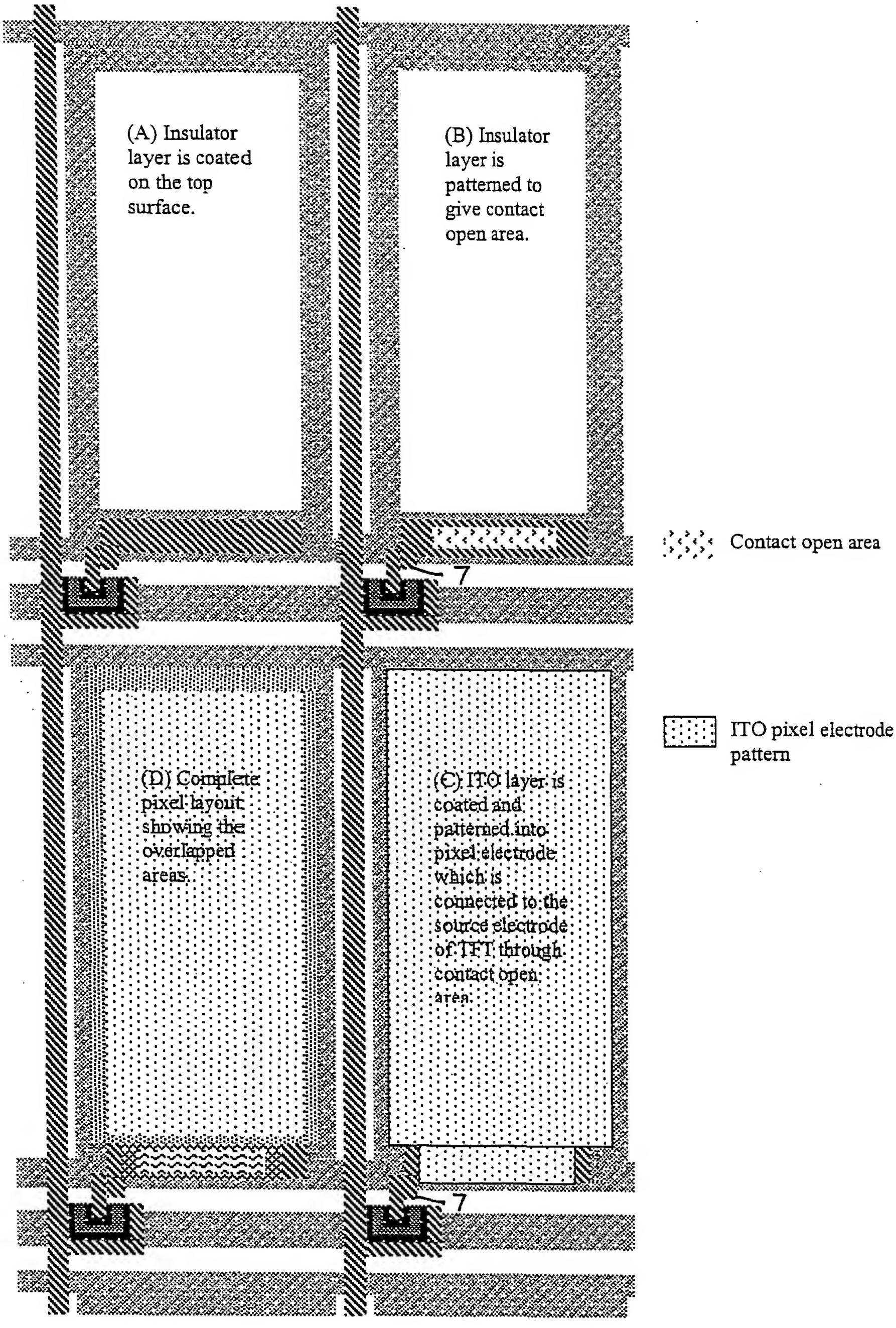
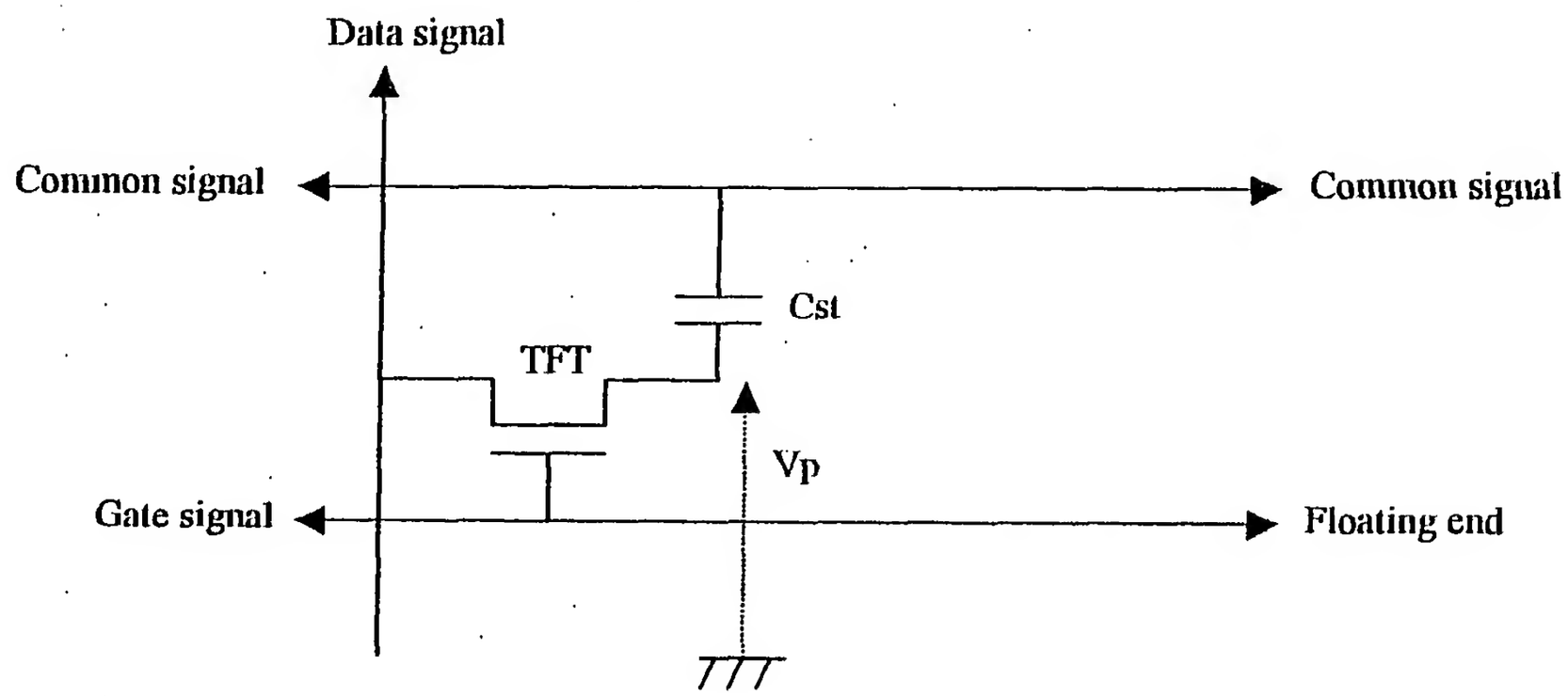


Figure 3. Simplified equivalent circuit of one cross point in TFT array.



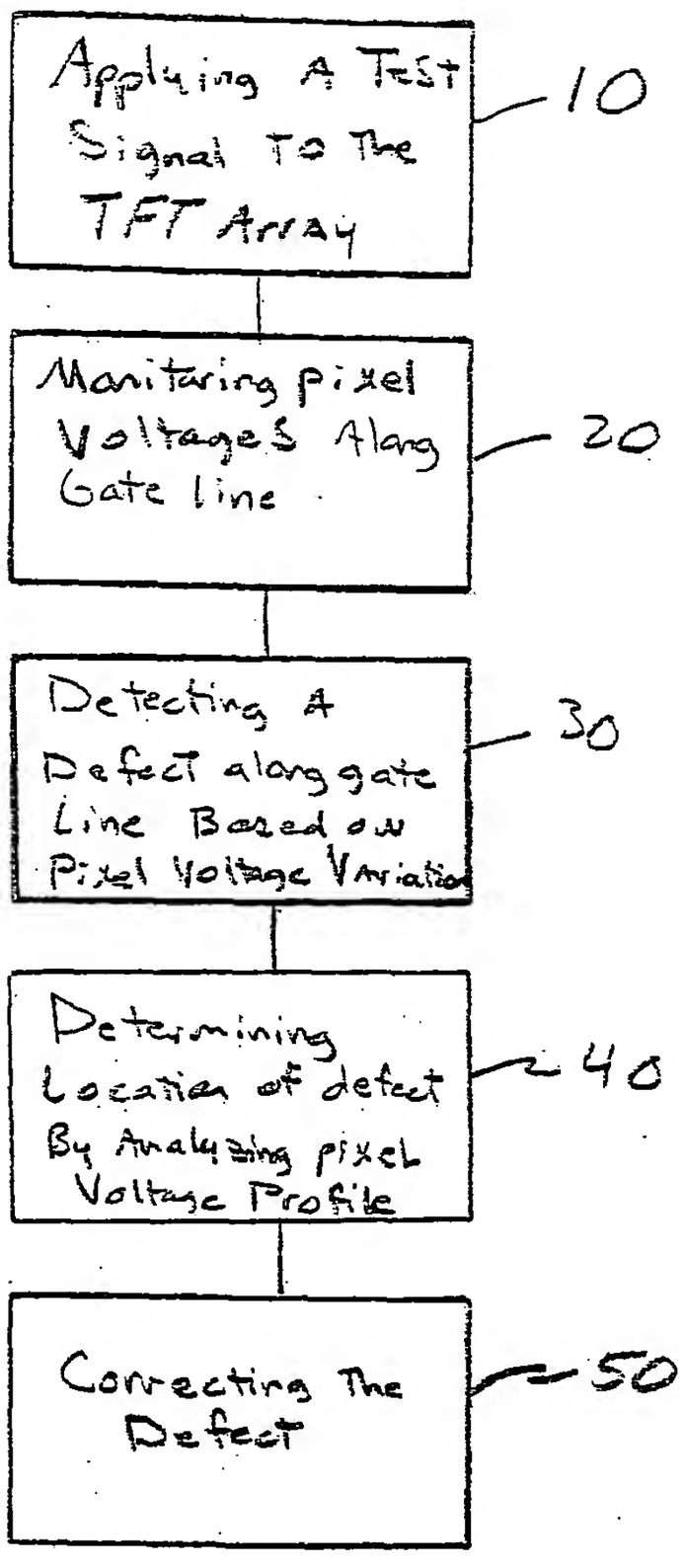

Applying A Test Signal To The TFT Array
10
Monitoring pixel Voltages Along Gate line
20
Detecting A Defect along gate Line Based on Pixel Voltage Variation
30
Determining Location of defect By Analyzing pixel Voltage Profile
40
Correcting The Defect
50

Fig. 3

Signal patterns to detect the short defect between gate and common lines.

Fig. 4 (a) Signal patterns for positive pixel voltage

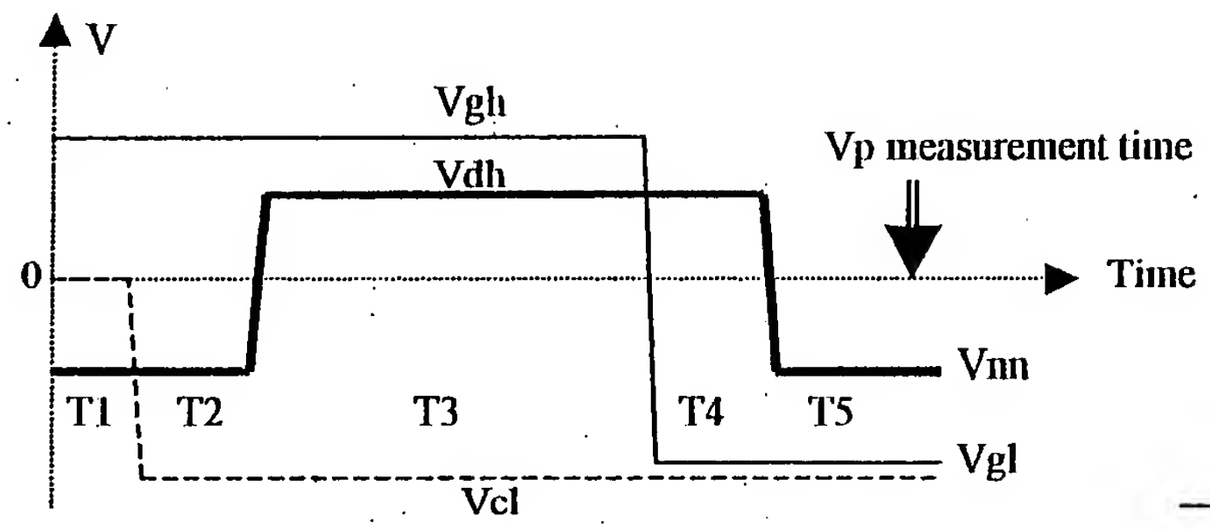
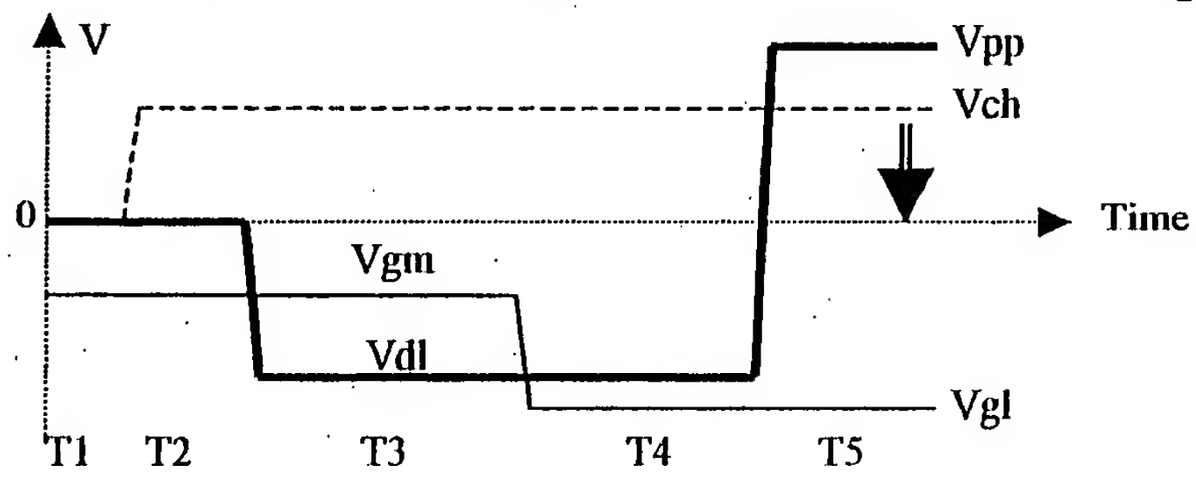


Fig. 4 (b) Signal patterns for negative pixel voltage



Gate signal

Data signal

Common signal

Figure 4. Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 2 (a) is applied.

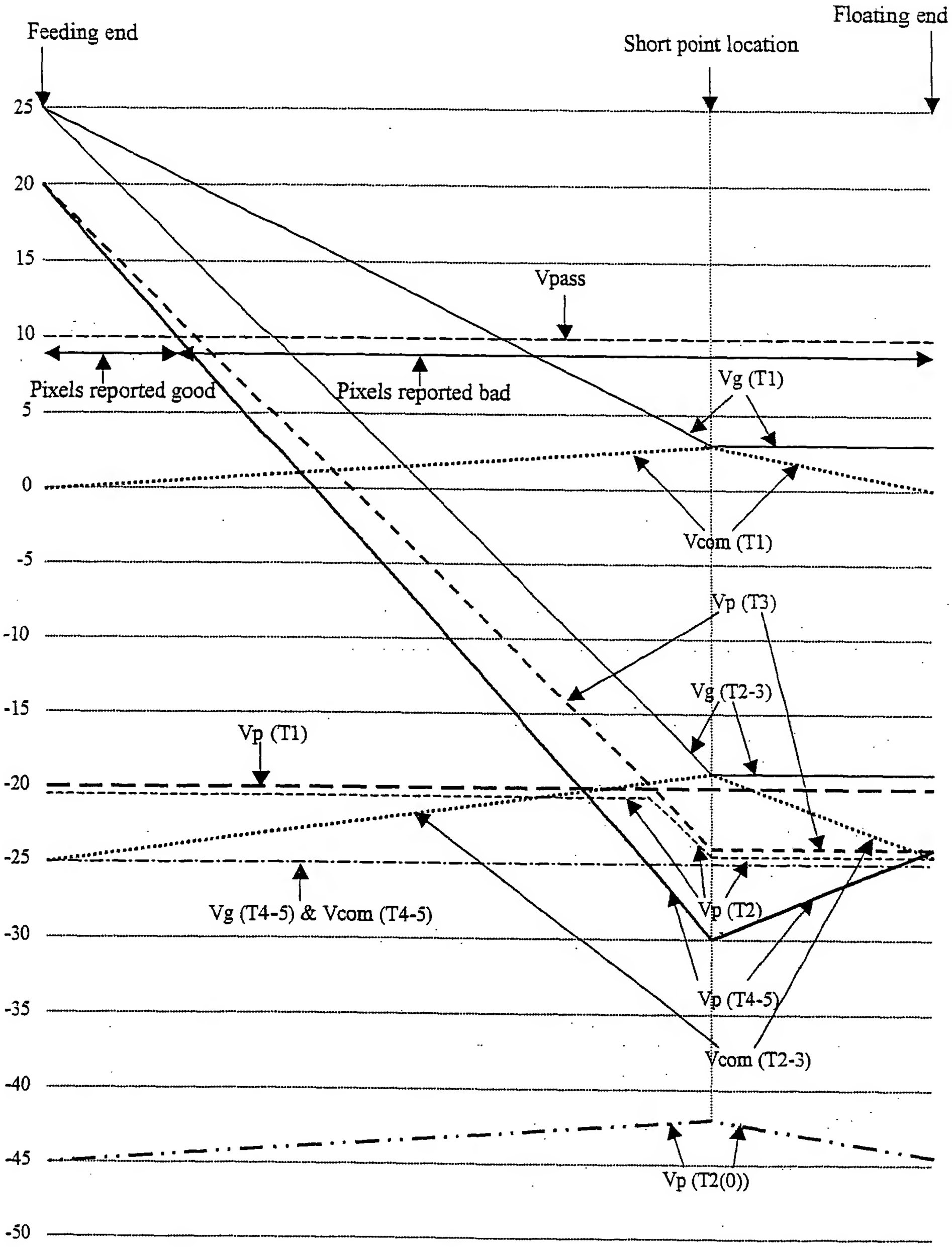


Figure 5. Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 2 (b) is applied.

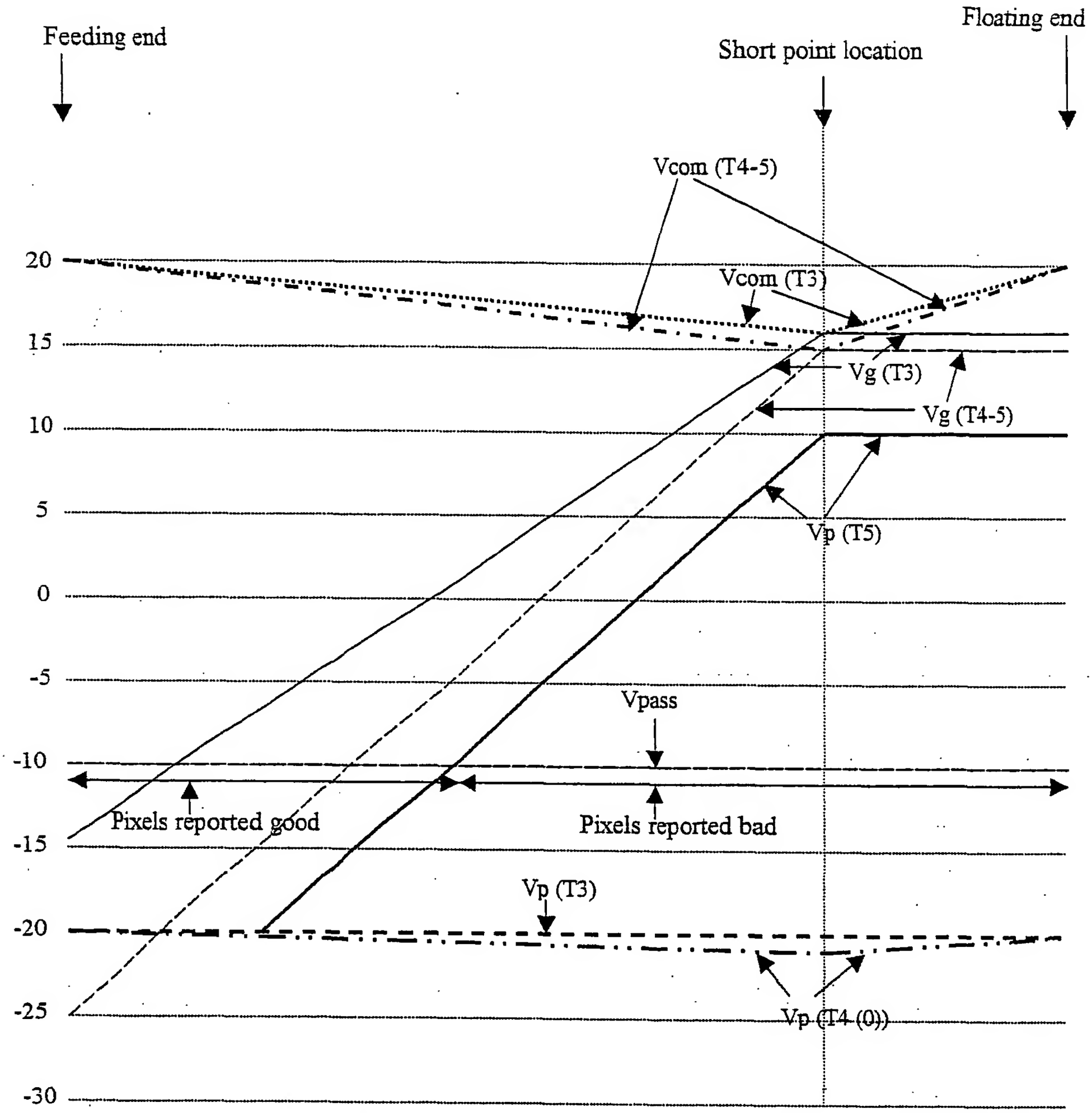


Figure 7: Calculation of pixel voltages (Vp (T4-5) of Fig 4 – Vp (T5) of Fig 5) along the gate line with a short defect between gate and self-common lines.

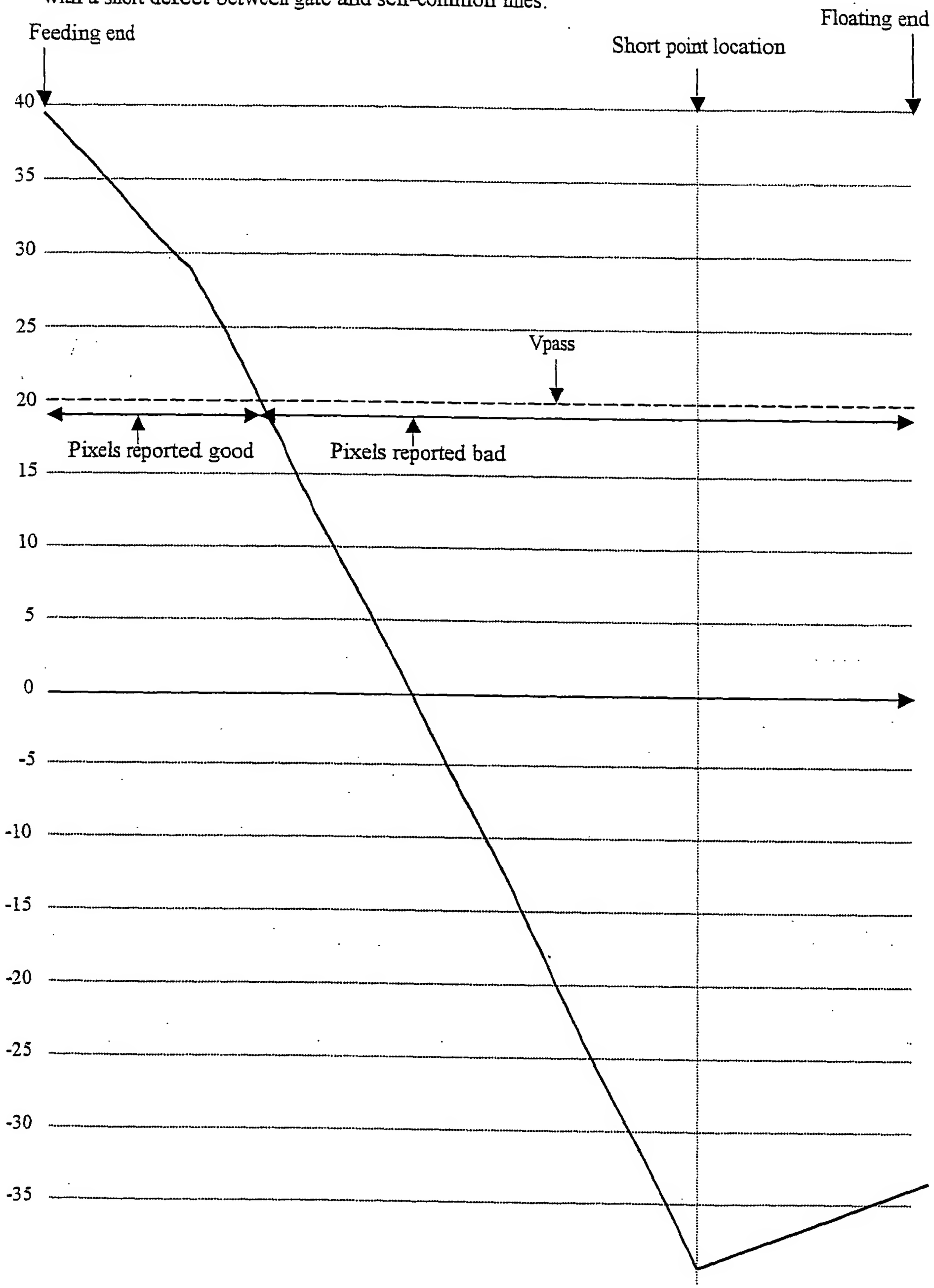


Figure 7. Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of Fig. 2 (a) is applied.

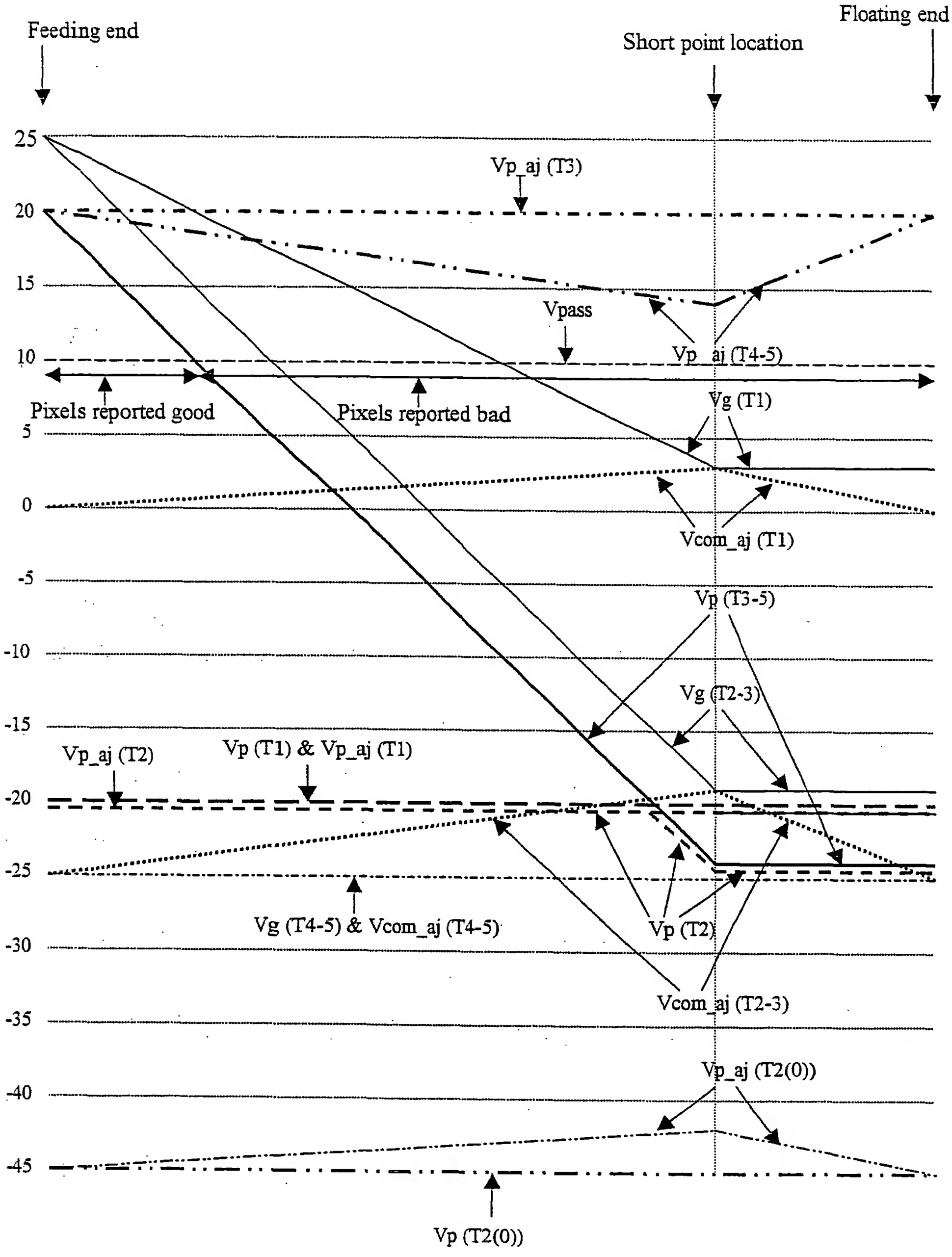


Figure 8. Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of Fig. 2 (b) is applied.

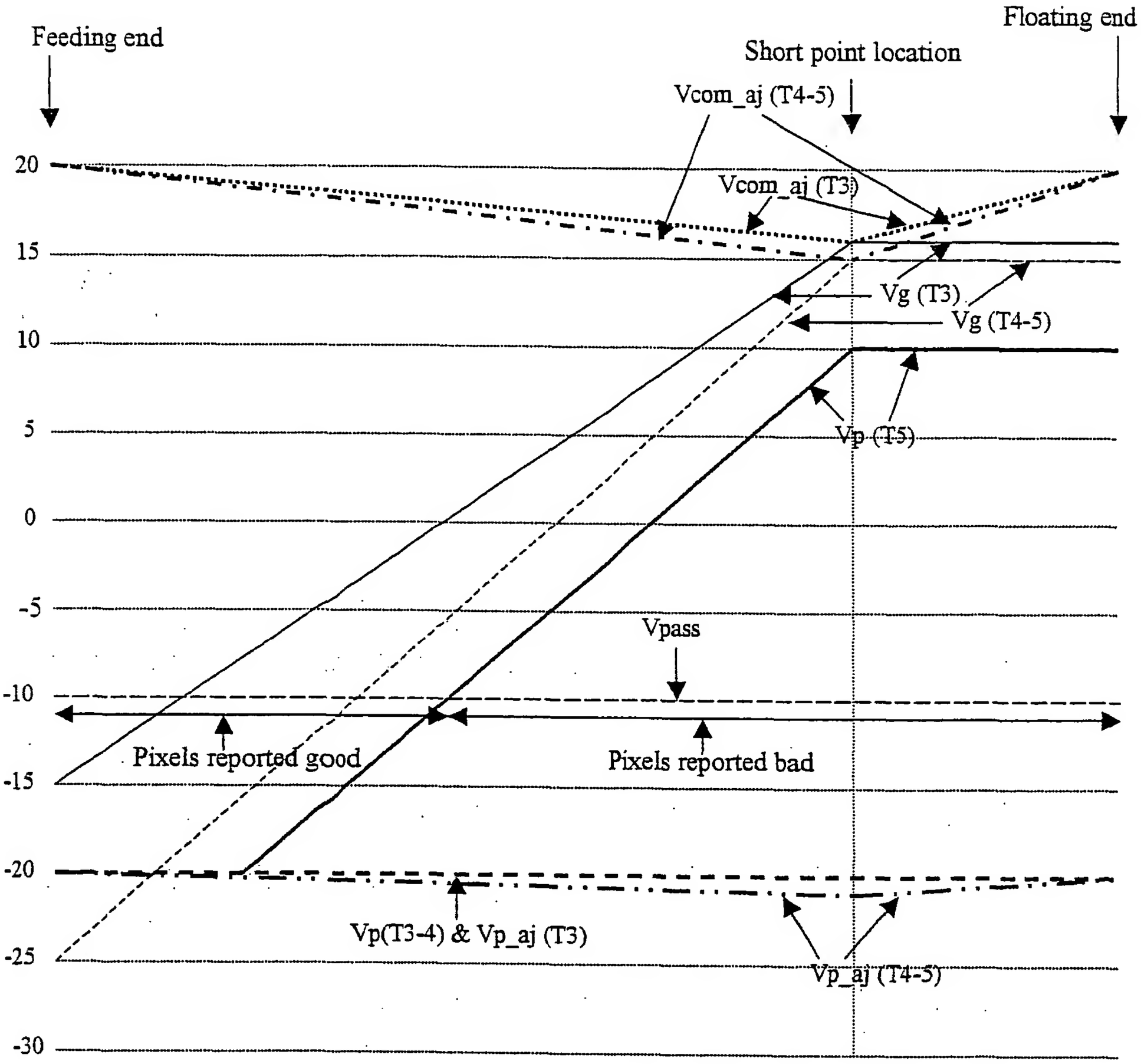
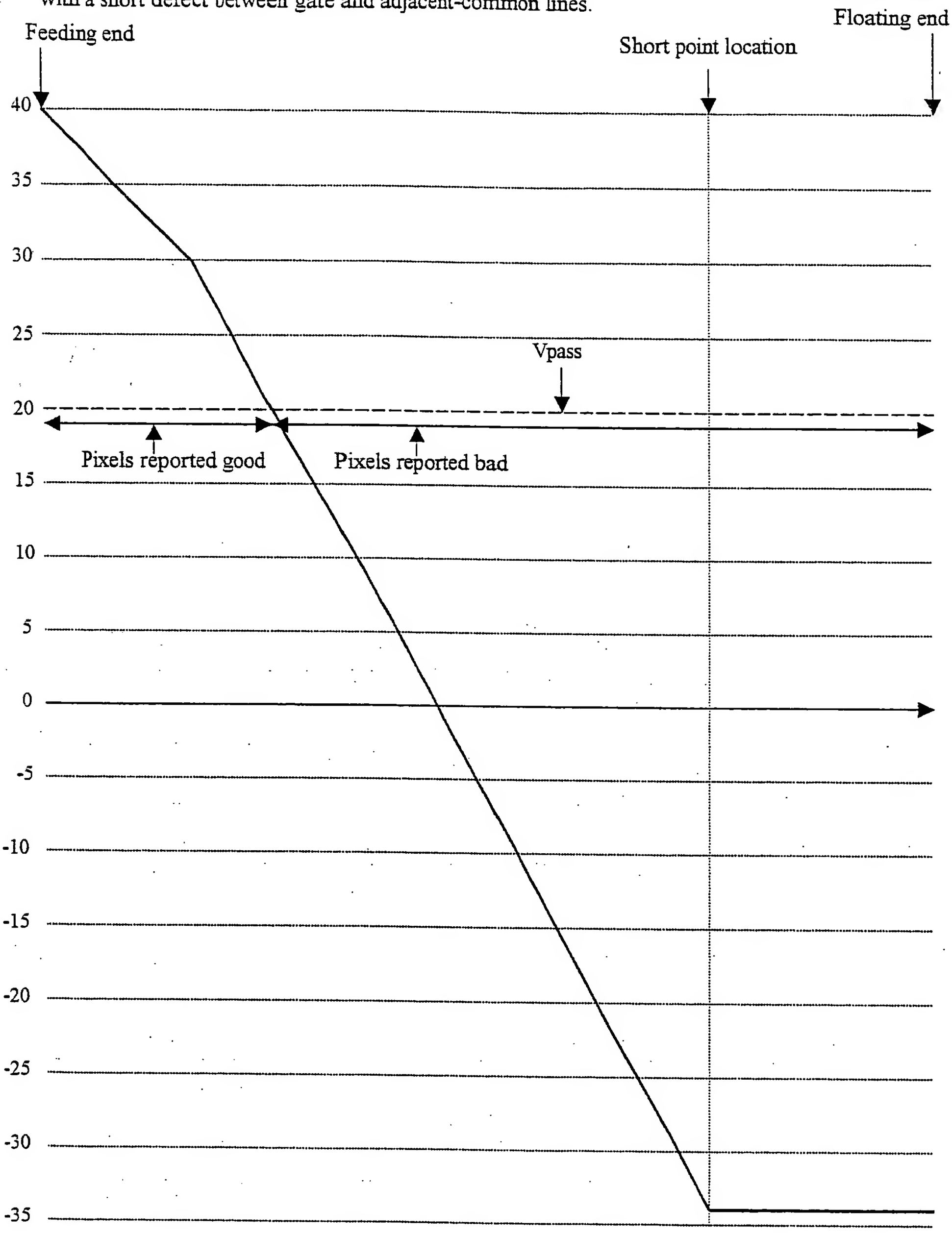


Figure 9. Calculation of pixel voltages (Vp (T3-5) of Fig 7 – Vp (T5) of Fig 8) along the gate line with a short defect between gate and adjacent-common lines.



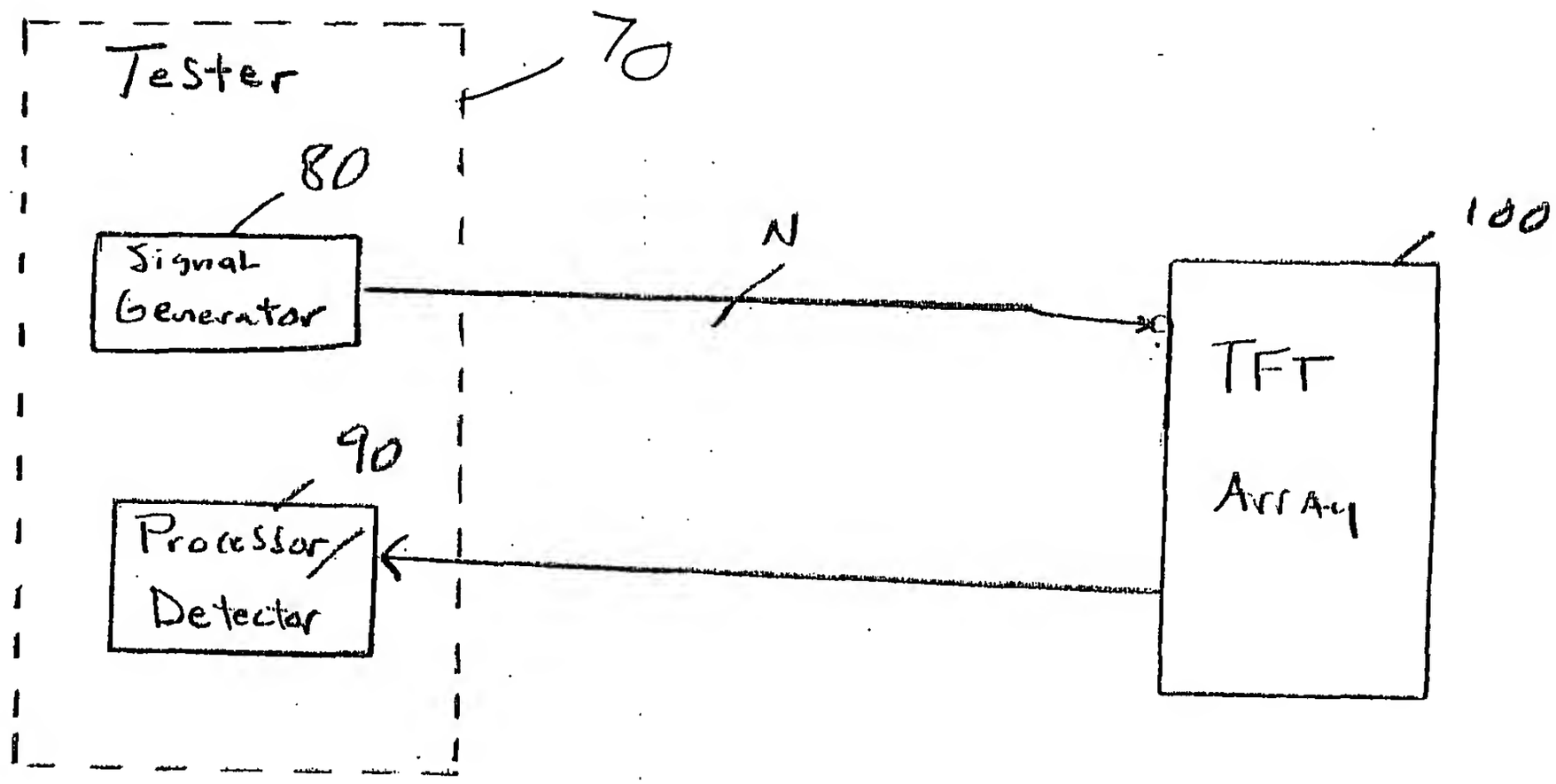

Tester
70
80
Signal Generator
N
100
TFT Array
90
Processor/ Detector

Fig. 11

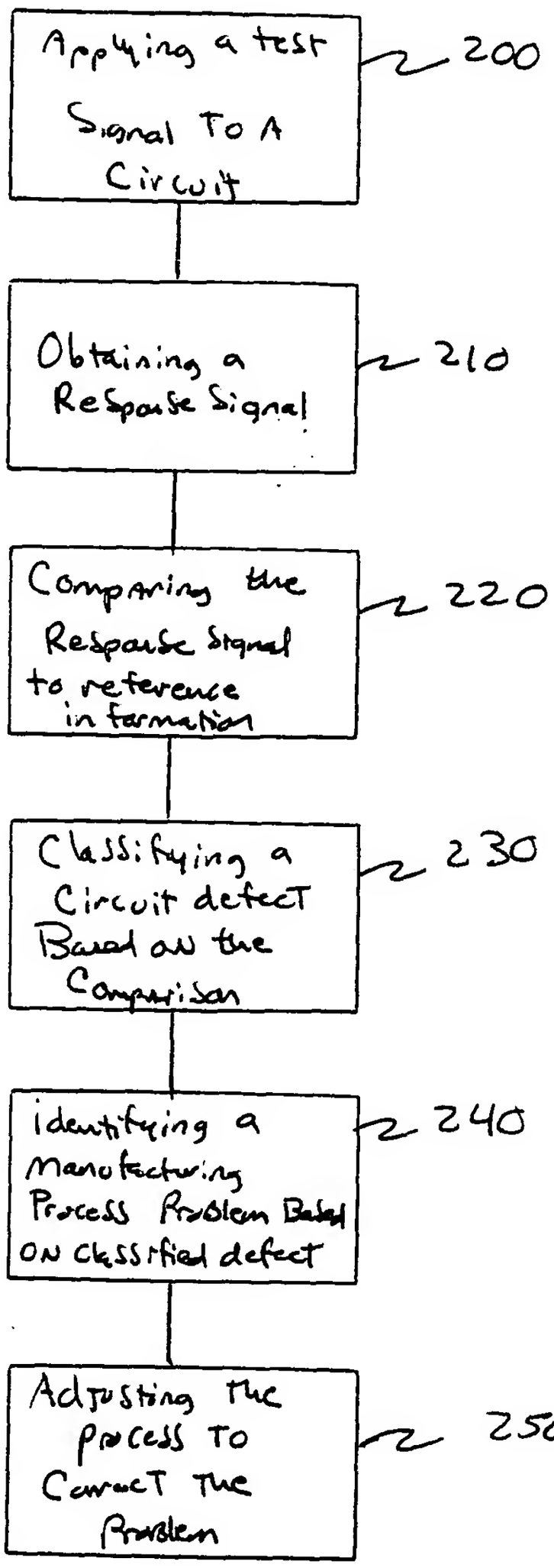
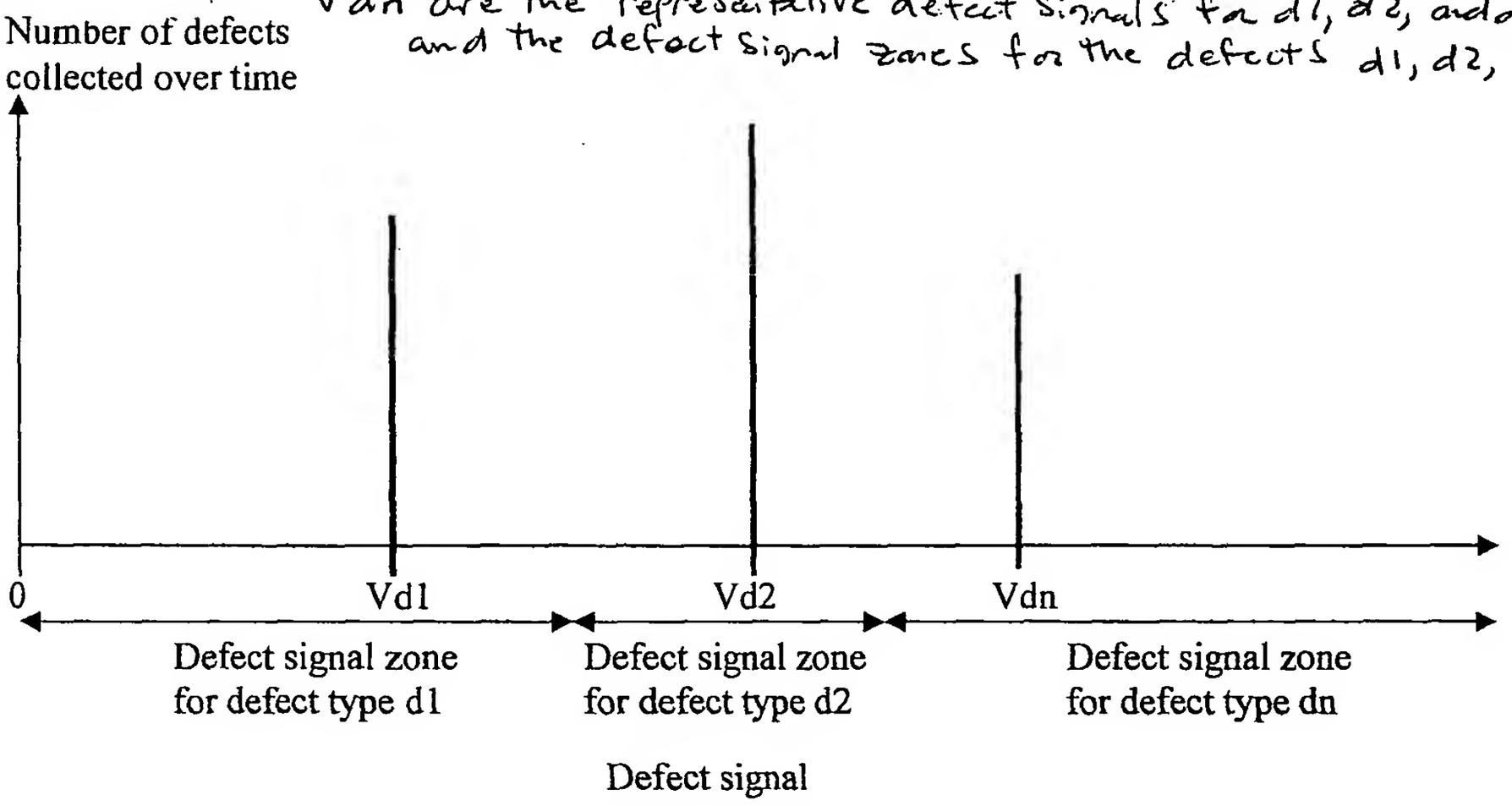

Applying a test Signal To A Circuit
200
Obtaining a Response Signal
210
Comparing the Response Signal to reference information
220
Classifying a Circuit defect Based on the Comparison
230
identifying a Manufacturing Process Problem Based ON classified defect
240
Adjusting the process To Correct the Problem
250

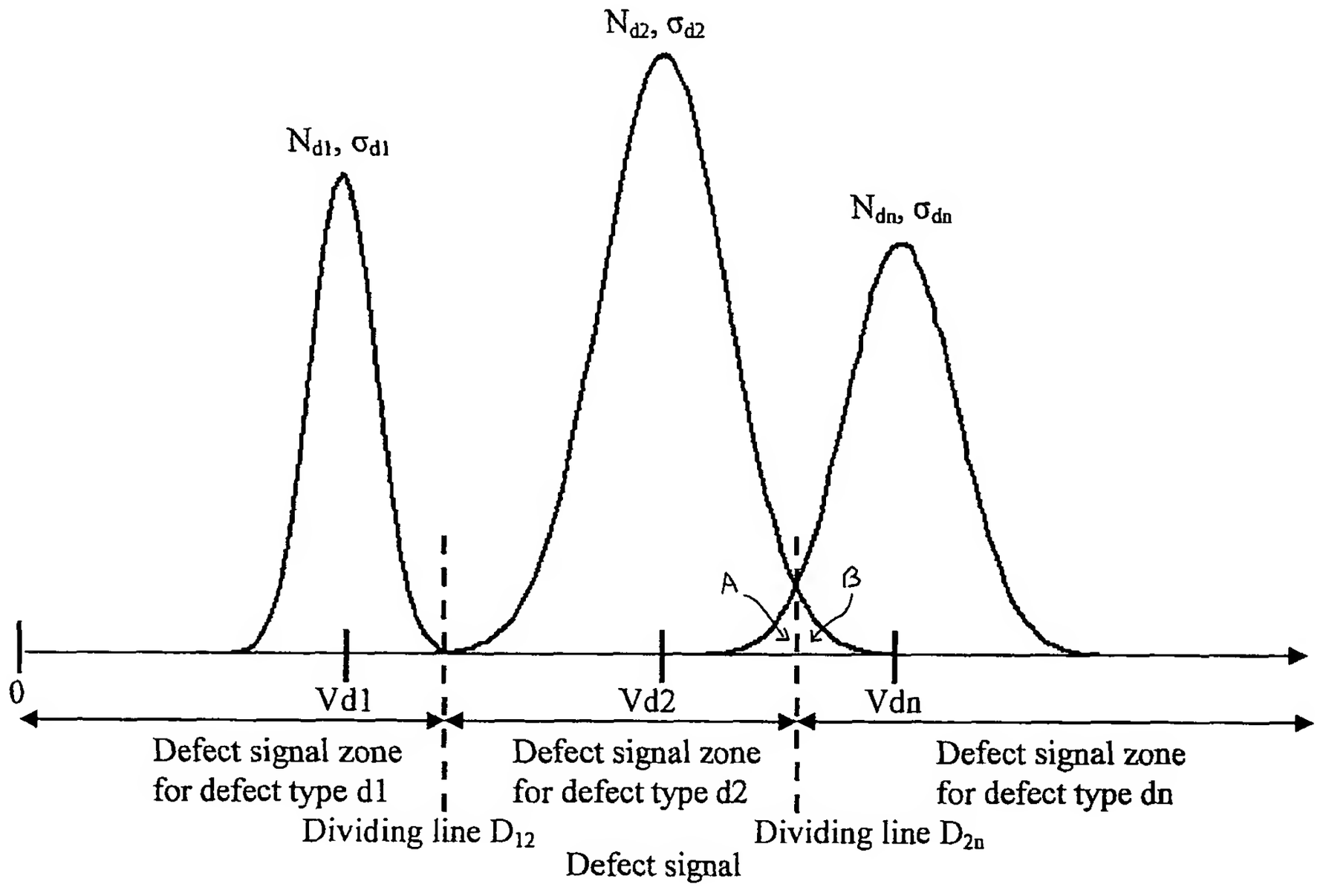
Figure 12

Fig. 13. Defect Histogram that was obtained using Ideal Distribution of defect signals For defects d1, d2, and dn, where Vd1, Vd2, and Vdn are the representative defect signals for d1, d2, and dn respectively and the defect signal zones for the defects d1, d2, and dn.



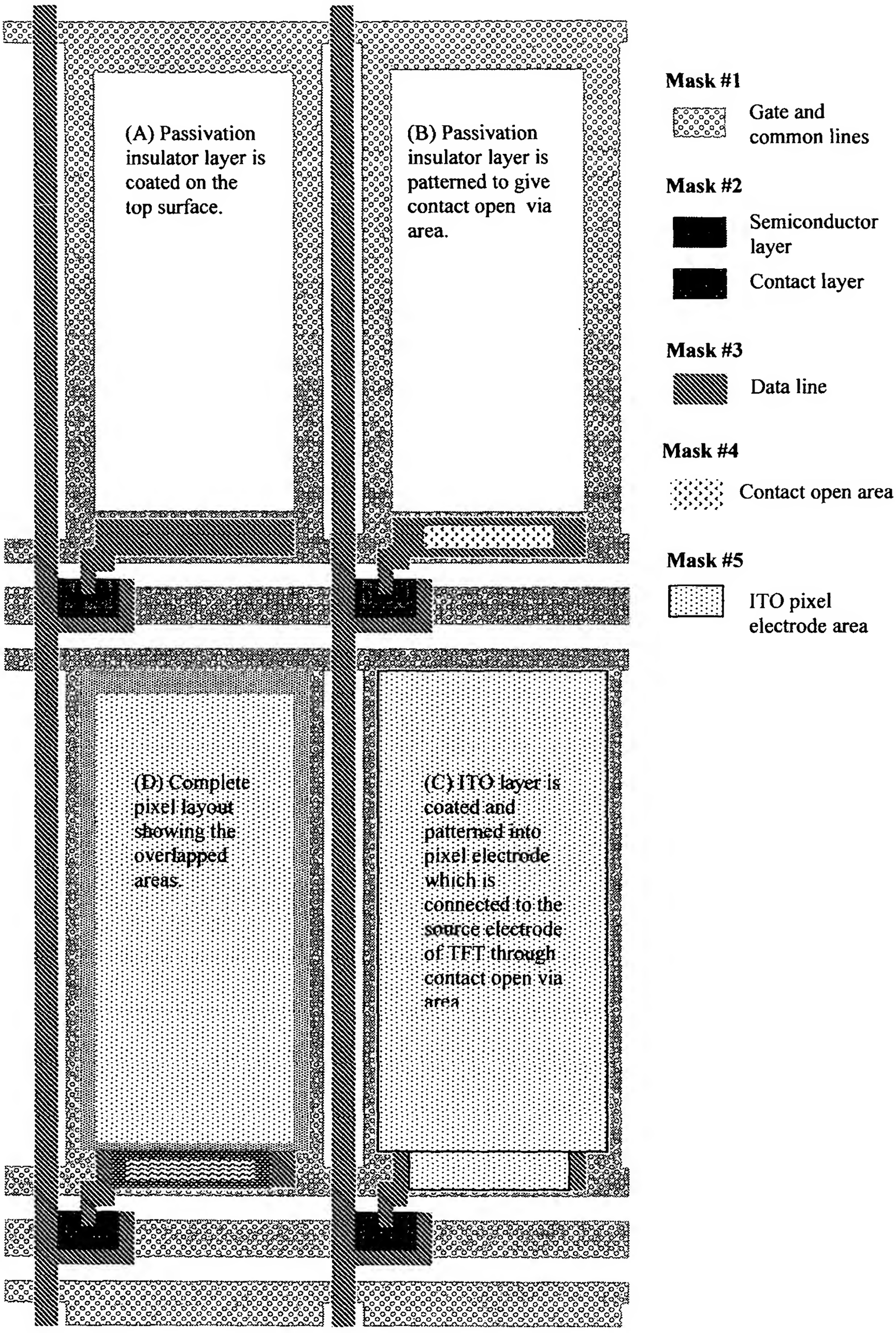
14

Figure ~~2~~. Realistic distribution of the defect signals for the defects d1, d2, and dn, where normal distribution function is used for each defect type.



15

Figure 3~~(b)~~. Explanation of pixel layout by showing four pixels in different process step.



16

Figure 4. Example of the process flow for TFT-array in Fig. 3.